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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,767	04/20/2001	Joachim Held	GR 00 P 1781	2019
7590 11/07/2005			EXAMINER	
LERNER AND GREENBERG, P.A. PATENT ATTORNEYS AND ATTORNEYS AT LAW Post Office Box 2480 Hollywood, FL 33022-2480			LE, DINH THANH	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary****(Supplemental)**

Application No.

09/839,767

Applicant(s)

HELD ET AL.

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6,8 and 10-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6,8 and 10-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**FINAL REJECTION (SUPPLEMENTAL)**

The applicant argues during the telephone conversation that the outstanding Office has not considered the limitation “the integrated circuit is a microprocessor or a microcontroller” newly added to claim 1 because it does not give a patentable weight. The argument is persuasive. A supplemental Office action necessitated to address this limitation as below:

***Claim Rejections - 35 USC § 112***

Claims 1-6, 8 and 10-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, it is unclear what the “microprocessor” and “microcontroller” is since they are not clearly defined.

The remaining claims are dependents from the above rejected claim and therefore also considered indefinite.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8 and 10-17 are rejected under 35 USC 102 (b) as being anticipated by Ikuta et al (US 5,789,797).

Ikuta et al discloses in Figures 1-2, 4-5, 11-12 and 17 an integrated circuit (3) comprising:

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- a first line (43) and a second line (45) for carrying DC voltages (VCC, ground) and low frequency voltages (interference noise), see lines 10-17, column 4;
- a radio-frequency filter device (14) having a first and second capacitors (C1, C2) connected to said lines and being completely integrated circuit for preventing and restricting a propagation of high-interference signals through said lines;
- wherein the integrated circuit (3) is interpreted as a microcontroller or a microprocessor because it performs the functions of sensing, controlling and processing.

With regard to claims 2 and 4-6, the recitation “component parts” is read on “circuit” in Figure 12.

With regard to claim 3, the recitation “component parts” for generating noise is read on box (21) in Figure 5.

With regard to claim 8, 10-11, 14, the recitation “resistor” is read on element (Rf in Figure 6 or R2 in Figure 12).

With regard to claim 12, the power (VCC) of Ikuta et al can be drawn completely from the first capacitor (C1).

With regard to claim 13, the current from the power (VCC) flowing through the resistor (Rf, R2) maintains the first capacitor (C1) continually charged and drawn completely from the first capacitor (C1).

With regard to claim 14, the filter (14) filters interference noise so that it does not interfere the operation of the integration circuit.

With regard to claim 16, the resistor (Rf, R2) inherently converts the interference noise partially into heat.

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With regard to claim 17, the recitation “plurality RF filter devices” and “component parts” are read on filter circuits (41, 42) and “circuits (9, 10), respectively.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6, 8 and 10-17 are rejected under 35Usc 103 (a) as being unpatentable over Oishi (US 6,331,719) in view of Ikuta et al (US 5,789,797).

Oishi discloses in figure 3-7 an integrated circuit (5) comprising:

- a first line (101) and a second line (109) for carrying DC voltages (VCC, ground) and low frequency voltages (interference noise) from a circuit (21);
- a radio-frequency filter device (107, 114) having a first capacitor (107) connected to said lines and being completely integrated circuit for preventing and restricting a propagation of high-interference signals through said lines; and

wherein the integrated circuit (5) is interpreted as “microcontroller” or “microprocessor” circuit because it includes circuits (21, 23) for performing the functions of controlling and processing..

With regard to claims 2 and 4-6, the recitation “component parts” is read on box (23).

With regard to claim 3, the recitation “component parts” for generating nose is read on a box (21) in Figure 3.

With regard to claim 8 and 10, the recitation “resistor” is read on element (105) in Figure 4.

With regard to claim 12, the component parts (23) coupled to the power (VCC) which can be drawn completely from the first capacitor (107).

With regard to claim 13, the current from the power (VCC) flowing through the resistor (105) maintains the first capacitor (107) continually charged and drawn completely from the first capacitor (107).

With regard to claim 16, the resistor (105) inherently converts the interference noise partially into heat because the interference noise is not allowed to pass through the filter.

With regard to claim 17, the recitation “plurality of RF filter device” and “component parts” are read on the filters 107, 114) and the boxes (21, 23), respectively.

However, Ooishi does not disclose that the filter comprising a second resistor and a second capacitor connected to said lines. For example, Ooishi employ a *first order* filter circuit including one resistor (105) and one capacitor (107) as shown in Figure 4. Ikuta et al teaches a second order low pass filter circuit in Figures 11-12 comprising two resistors (R1, R2) and two capacitors (C1, C2) coupled between lines for effectively removing all of high frequency noise. It would have been obvious to a person having skill in the art at the time the invention was made to employ the second order filter as suggested by Ikuta et al in the circuit of Ooishi for the purpose of effectively removing all of high frequency noise. Also, as well known in the filter art, the number of the order of a filter determines the bandwidth of the filter pass-band or the stiffness of the roll-off region below the 3 dB cutoff point. Example, the amplitude of noise signals when they pass through a filter having a high order would be attenuated more than when

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the signals pass through the same filter with a lower order. Since the circuit of Ooishi must be employed within a predetermined system, obviously, its specification should be accommodated with the requirement of the predetermined system. Thus, employing a second order filter in the circuit of Ooishi for providing a high attenuation within the roll-off region is considered to be a matter of a design expedient for an engineer. It would have been obvious to a person having skill in the art at the time the invention was made to employ the second order in the circuit of Ooishi for the purpose of providing a high attenuation within the roll-of region to lower the noise level so that the noise would not degrade the predetermined system.

### ***Response to Applicant's Arguments***

The applicant argues that the integrated circuit of Ikuta and Ooishi is a microprocessor or a microcontroller, in particular, Fig. 17 of Ikuta includes in the sensor chip 3 a block entitled "processing circuit" which is a combination of the first circuit 9 and the second circuit 10 of Figs. 1 and 4 of Ikuta. The argument is not persuasive because the integrated circuit (3) of Ikuta is interpreted as a microcontroller or a microprocessor circuit because it performs the functions of sensing and processing. The integrated circuit (5) of Ooishi et al is also interpreted as "microcontroller" or "microprocessor circuit" because it performs the functions of controlling and processing.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**DINH T. LE**  
**PRIMARY EXAMINER**